Wednesday, August 29th

Wednesday - ROOM 1

MAIN **DSD 2018** ***MEMORY***
Chair: **Shen-Fu Hsiao**
Session Duration: **11:45-13:15**

	[START-TIME]	[END-TIME]	
55	11:45	12:15	**Memory Aware Packet Matching Architecture for High-Speed Networks** *Michal Kekely, Lukáš Kekely and Jan Korenek*
135	12:15	12:45	**Real-time Emulation of Multiple NAND Flash Channels by Exploiting the DRAM Memory of High-end Servers** *Nikolaos Toulgaridis, Eleni Bougioukou and Theodore Antonakopoulos*
106	12:45	13:15	**High-Speed Configuration Strategy for Configurable Logic Block-based TCAM Architecture on FPGA** *Inayat Ullah, Umar Afzaal, Zahid Ullah and Jeong-A Lee*

MAIN **DSD 2018** ***ARCHITECTURE/ARITHMETICS/COMPUTING***
Chair: **Francisco-Javier Veredas**
Session Duration: **14:30-16:30**

	[START-TIME]	[END-TIME]	
96	14:30	15:00	**Architectural Exploration of Function Computation Based on Cubic Polynomial Interpolation with Application in Deep Neural Networks** *Shen-Fu Hsiao, Hsian-Hao Lian and Yu-Chang Chen*
62	15:00	15:30	**Measurement Based Execution Time Analysis of GPGPU Programs via SE+GA** *Adrian Horga, Sudipta Chattopadhyay, Petru Eles and Zebo Peng*
71	15:30	15:50	**Heavy-hitter detection using a hardware sketch with the Countmin-CU algorithm** *Antonio Saavedra, Cecilia Hernandez and Miguel Figueroa*
143	15:50	16:10	**A Novel Hardware-Accelerated Priority Queue for Real-Time Systems** *Lukas Kohutka, Lukas Nagy and Viera Stopjakova*
30	16:10	16:30	**Datawidth-Aware Energy-Efficient Multipliers: A Case for Going Sign Magnitude** *Luc Waeijen, Yifan He, Hailong Jiao and Henk Corporaal*

MAIN **DSD 2018** ***CHIP DESIGN***
Chair: **Miguel Figueroa**
Session Duration: **17:00-18:30**

	[START-TIME]	[END-TIME]	
93	17:00	17:30	**Invited talk - Trends in On-Chip Dynamic Resource Management** *Kasra Moazzemi, Anil Kanduri, David Juhasz, Antonio Miele, Amir M. Rahmani, Pasi Liljeberg, Axel Jantsch and Nikil Dutt*
41	17:30	17:50	**FPGA Placement Improvement Using a Genetic Algorithm and the Routing Algorithm as a Cost Function** *Francisco Javier Veredas and Enrique J. Carmona Suárez*
48	17:50	18:10	**Fault-Tolerant Deployment of Dataflow Applications Using Virtual Processors** *Reinier van Kampenhout, Sander Stuijk and Kees Goossens*
60	18:10	18:30	**Novel Feature Vectors Considering Distances between Wires for Lithography Hotspot Detection** *Gaku Kataoka, Masato Inagi, Shinobu Nagayama and Shin'Ichi Wakabayashi*

Wednesday - ROOM 2

DTFT **Dependability, Testing and Fault Tolerance in Digital Systems**
Chair: **Jan Schmidt**
Session Duration: **11:45-13:15**

	[START-TIME]	[END-TIME]	
126	11:45	12:15	**DUSTER: Dual Source Write Termination Method for STT-RAM Memories** *Saeed Seyed Faraji, Javad Talafy, Amir Mohammad Hajisadeghi and Hamid Zarandi*
119	12:15	12:35	**Error Correctable Approximate Multiplier With Area/Power Efficient Design through Mixed CMOS/PTL** *Tooba Arifeen, Abdus Sami Hassan and Jeong-A Lee*
13	12:35	12:55	**Effect of FPGA Circuit Implementation on Error Detection Using Logic Implication Checking** *Umar Afzaal, Abdus Sami Hassan, Tooba Arifeen and Jeong-A Lee*
69	12:55	13:15	**D-SET Mitigation Using Common Clock Tree Insertion Techniques for Triple-Clock TMR Flip-Flop** *Oliver Schrape, Anselm Breitenreiter, Marko Andjelkovic and Milos Krstic*

DTFT **Dependability, Testing and Fault Tolerance in Digital Systems**
Chair: **Petr Fišer**
Session Duration: **14:30-16:30**

	[START-TIME]	[END-TIME]	
38	14:30	14:50	**Optimal Dependability and Fine Granular Error Resilience Methodology for Reconfigurable Systems** *Farnoosh Hosseinzadeh, Petr Pfeifer and Heinrich T. Vierhaus*
100	14:50	15:10	**Program Generation Through a Probabilistic Constrained Grammar** *Ondrej Cekan, Zdenek Kotasek and Jakub Podivinsky*
109	15:10	15:30	**A Generic Methodology to Compute Design Sensitivity to SEU in SRAM-based FPGA** *Mahsa Mousavi, Hamid Reza Pourshaghaghi, Mohammad Tahghighi, Roel Jordans and Henk Corporaal*
65	15:30	15:50	**Evaluation Platform for Testing Fault Tolerance Properties: Soft-core Processor-based Experimental Robot Controller** *Jakub Podivinsky, Jakub Lojda, Ondrej Cekan and Zdenek Kotasek*
133	15:50	16:10	**MOMENT: A Cross-Layer Method to Mitigate Multiple Event Transients in Combinational Circuits** *Amir Mohammad Hajisadeghi, Hossein Bardareh and Hamid Zarandi*
81	16:10	16:30	**FT-EST Framework: Reliability Estimation for the Purposes of Fault-Tolerant System Design Automation** *Jakub Lojda, Jakub Podivinsky, Ondrej Cekan, Richard Panek and Zdenek Kotasek*

ASAASIT **Architectures and Systems for Automotive, Aeronautic, Space and Intelligent Transportation**
Chair: **Hamid Reza-Pourshaghaghi**
Session Duration: **17:00-18:30**

	[START-TIME]	[END-TIME]	
11	17:00	17:30	**A Hypervisor Architecture for Low-Power Real-Time Embedded Systems** *Tomaso Poggi, Peio Onaindia, Mikel Azkarate-Askatsua, Kim Gruttner, Maher Fakih, Salvador Peiró and Patricia Balbastre*
58	17:30	18:00	**Segmentation of hyperspectral images using quantized convolutional neural networks** *Pablo Ribalta Lorenzo, Michal Marcinkiewicz and Jakub Nalepa*
140	18:00	18:30	**Design of a Low-Level Radar and Time-of-Flight Sensor Fusion Framework** *Josef Steinbaeck, Norbert Druml, Gerald Holweg and Christian Steger*

Wednesday - ROOM 3

DCPS **Design of Cyber-Physical Systems**
Chair: **Dip Goswami**
Session Duration: **11:45-13:15**

	[START-TIME]	[END-TIME]	
160	11:45	12:15	**Invited talk - Intelligent Security Measures for Smart Cyber Physical Systems** *Muhammad Shafique, Faiq Khalid and Semeen Rehman*
153	12:15	12:45	**Designing Energy Efficient Approximate Multipliers for Neural Acceleration** *Sayandip De, Jos Huisken and Henk Corporaal*
72	12:45	13:15	**Resource-aware Decentralization of a UKF-based Cooperative Localization for Networked Mobile Robots** *Seyyed Ahmad Razavi, Eli Bozorgzadeh, Solmaz Kia and Kanghee Kim*

AMDL **Applications, Architectures, Methods and Tools for Machine- and Deep Learning**
Chair: **Henk Corporaal**
Session Duration: **14:30-16:30**

	[START-TIME]	[END-TIME]	
162	14:30	15:00	**Quantization of constrained processor data paths applied to Convolutional Neural Networks** *Barry de Bruin, Zoran Zivkovic and Henk Corporaal*
35	15:00	15:30	**CoNNA – Compressed CNN Hardware Accelerator** *Rastislav Struharik, Bogdan Vukobratović, Andrea Erdeljan and Damjan Rakanović*
168	15:30	15:50	**Run-time Mapping Algorithm for Dynamic Workloads on Heterogeneous MPSoCs Platforms** *Sima Sinaei and Omid Fatemi*
172	15:50	16:10	**FPGA Based Reconfigurable Coprocessor for Deep Convolutional Neural Network Training** *Sajna Remi Clere, Sachin S and Kuruvilla Varghese*
141	16:10	16:30	**Generation of a Diagnosis Model for Hybrid-Electric Vehicles using Machine Learning** *Simon Meckel, Roman Obermaisser and Jie-Uei Yang*

AMDL **Applications, Architectures, Methods and Tools for Machine- and Deep Learning**
Chair: **Maurice Peemen**
Session Duration: **17:00-18:30**

	[START-TIME]	[END-TIME]	
175	17:00	17:30	**ADONN: Adaptive Design of Optimized Deep Neural Networks for Embedded Systems** *Mohammad Loni, Masoud Daneshtalab and Mikael Sjödin*
155	17:30	18:00	**Embedded Real-Time Fall Detection with Deep Learning on Wearable Devices** *Emanuele Torti, Alessandro Fontanella, Mirto Musci, Nicola Blago, Danilo Pau, Francesco Leporati and Marco Piastra*
9	18:00	18:30	**A Machine Learning Approach for Area Prediction of Hardware Designs from Abstract Specifications** *Elena Zennaro, Lorenzo Servadei, Keerthikumara Devarajegowda and Wolfgang Ecker*

Thursday, August 30th

Thursday - ROOM 1

MAIN **DSD 2018** ***IMAGE PROCESSING/CODING***
Chair: **Amir Rahmani**
Session Duration: **11:45-13:15**

	[START-TIME]	[END-TIME]	
92	11:45	12:15	**Multimodal image registration between SWIR and LWIR images in an embedded system** *Javier Cardenas and Miguel Figueroa*
129	12:15	12:35	**A Reconfigurable Fractional Interpolation Hardware for FVC Motion Compensation** *Hasan Azgin, Ahmet Can Mert, Ercan Kalali and Ilker Hamzaoglu*
121	12:35	12:55	**Memory-Centric Flooded LDPC Decoder Architecture Using Non-Surjective Finite Alphabet Iterative Decoding** *Oana Boncalo, Alexandru Amaricai and Sergiu Nimara*
10	12:55	13:15	**High-throughput one-channel RS(255,239) Decoder** *Gabriele Perrone, Javier Valls, Vicente Torres and Francisco Garcia-Herrero*

ASHWPA **Advanced Systems in Healthcare, Wellness and Personal Assistance**
Chair: **Francesco Leporati**
Session Duration: **14:30-16:30**

	[START-TIME]	[END-TIME]	
117	14:30	15:00	**Self-Aware Wearable Systems in Epileptic Seizure Detection** *Farnaz Forooghifar, Amir Aminifar and David Atienza Alonso*
114	15:00	15:30	**Exploring the usage of Time-of-Flight Cameras for contact and remote Photoplethysmography** *Caterina Nahler, Bernhard Feldhofer, Gerald Holweg and Norbert Druml*
118	15:30	15:50	**The Accuracy and Efficacy of Realtime Compressed ECG Signal Reconstruction on a Heterogeneous Multicore Edge-Device** *Mohammed Al Disi, Hamza Djelouat, Abbes Amira and Faycal Bensaali*
77	15:50	16:10	**Virtual White Cane featuring Time-of-Flight 3D Imaging supporting Visually Impaired Users** *Norbert Druml, Thomas Pietsch, Markus Dielacher, Christian Steger, Marcus Baumgart, Cristina Consani, Thomas Herndl and Gerald Holweg*

Thursday - ROOM 2

AHSA **Architectures and Hardware for Security Applications**
Chair: **Paris Kitsos**
Session Duration: **11:45-13:15**

	[START-TIME]	[END-TIME]	
25	11:45	12:15	**Guards in Action: First-Order SCA Secure Implementations of Ketje without Additional Randomness** *Victor Arribas, Svetla Nikova and Vincent Rijmen*
85	12:15	12:45	**OpenSSL Bellcore's Protection Helps Fault Attack.** *Sébastien Carré, Matthieu Desjardins, Adrien Facon and Sylvain Guilley*
75	12:45	13:15	**Analysis of Mixed PUF-TRNG Circuit Based on SR-Latches in FD-SOI Technology** *Jean-Luc Danger, Risa Yashiro, Tarik Graba, Sylvain Guilley, Yves Mathieu, Noriyuki Miura, Abdelmalek Si-Merabet, Kazuo Sakiyama and Makoto Nagata*

AHSA **Architectures and Hardware for Security Applications**
Chair: **Jean-Luc Danger and Robert Lorencz**
Session Duration: **14:30-16:30**

	[START-TIME]	[END-TIME]	
105	14:30	14:50	**An FPGA Hardware Trojan Detection Approach Based on Multiple Parameter Analysis** *Apostolos Fournaris, Lampros Pyrgas and Paris Kitsos*
73	14:50	15:10	**Dummy rounds as a DPA countermeasure in hardware** *Stanislav Jerabek, Jan Schmidt, Martin Novotny and Vojtech Miskovsky*
83	15:10	15:30	**CCFI-Cache: A Transparent and Flexible Hardware Protection for Code and Control-Flow Integrity** *Jean-Luc Danger, Adrien Facon, Sylvain Guilley, Karine Heydemann, Ulrich Kühne, Abdelmalek Si Merabet and Michael Timbert*
113	15:30	15:50	**Reliability Driven Mixed Critical Tasks Processing on FPGAs against Hardware Trojan Attacks** *Krishnendu Guha, Atanu Mazumder, Debasri Saha and Amlan Chakrabarti*
163	15:50	16:10	**Design of a fully balanced ASIC coprocessor implementing complete addition formulas on Weierstrass elliptic curves** *Niels Pirotte, Jo Vliegen, Lejla Batina and Nele Mentens*
18	16:10	16:30	**An Improved Analysis Of Reliability And Entropy For Delay PUFs** *Alexander Schaub, Jean-Luc Danger, Sylvain Guilley and Olivier Rioul*

Thursday - ROOM 3

DCPS **Design of Cyber-Physical Systems**
Chair: **Jos Huisken**
Session Duration: **11:45-13:15**

	[START-TIME]	[END-TIME]	
158	11:45	12:05	**Design Optimization of Cyber-Physical Systems by Partitioning and Coordination: A Study on Mechatronic Systems** *Pouya Mahdavipour Vahdati, Lei Feng and Martin Törngren*
21	12:05	12:25	**Stability Verification of Self-Timed Control Systems using Model-Checking** *Viktorio Hakim and Marco Bekooij*
91	12:25	12:45	**Optimising Quality-of-Control for Data-intensive Multiprocessor Image-Based Control Systems considering Workload Variations** *Sajid Mohamed, Diqing Zhu, Dip Goswami and Twan Basten*
70	12:45	13:05	**Circuit Inspired Modeling Method for Irrigation** *Davit Hovhannisyan, Ahmed Eltawil, Mohammad Al Faruque and Fadi Kurdahi*

EPDSD **European Projects in Digital System Design**
Chair: **Lech Jozwiak**
Session Duration: **14:30-16:30**

	[START-TIME]	[END-TIME]	
170	14:30	15:00	**Invited talk - Design and Implementation of a Privacy Framework for the Internet of Things (IoT)** *Paris Panagiotou, Nicolas Sklavos and Ioannis Zaharakis*
97	15:00	15:30	**Invited talk - The AQUAS ECSEL Project** *Luigi Pomante, Bohuslav Křena, Tomáš Vojnar, Filip Veljković and Pacôme Magnin*
110	15:30	16:00	**Invited talk - ANTAREX: A DSL-based Approach to Adaptively Optimizing and Enforcing Extra-Functional Properties in High Performance Computing** *Cristina Silvano, Giovanni Agosta, Andrea Bartolini, Andrea R. Beccari, Luca Benini, Loic Besnard, Joao Bispo, Radim Cmar, Joao M. P. Cardoso, Carlo Cavazzoni, Stefano Cherubin, Davide Gadioli, Martin Golasowski, Imane Lasri, Jan Martinovic, Gianluca Palermo, Pedro Pinto, Erven Rohou, Nico Sanna, Katerina Slaninova and Emanuele Vitali*
165	16:00	16:30	**Invited talk - A Review of Near-Memory Computing Architectures: Opportunities and Challenges** *Gagandeep Singh, Lorenzo Chelini, Stefano Corda, Ahsan Javed Awan, Sander Stuijk, Roel Jordans, Henk Corporaal and Albert-Jan Boonstra*

Friday, August 31st

Friday - ROOM 1

MAIN **DSD 2018** ***SIMULATION/MODELING/EDUCATION***
Chair: **Oana Boncalo**
Session Duration: **11:15-13:15**

	[START-TIME]	[END-TIME]	
95	11:15	11:45	**Invited talk - COSSIM: An Open-Source Integrated Solution to Address the Simulator Gap for Systems of Systems** *Andreas Brokalakis, Danilo Pau, Marco Marcon, Marco Paracchini, Emanuele Plebani, Yannis Papaefstathiou, Antonios Nikitakis, Nikolaos Tampouratzis, Stamatis Andrianakis, Ramakrishnan Geethakumari Prajith, Ioannis Sourdis, Maria Carmen Palacios, Miquel Angel Anton and Attila Szasz*
138	11:45	12:15	**Compositional Dataflow Modelling for Cyclo-Static Applications** *Hadi Alizadeh Ara, Marc Geilen, Amir Reza Baghban Behrouzian, Twan Basten and Dip Goswami*
152	12:15	12:35	**Timing prediction for service-based applications mapped on Linux-based multi-core platforms** *Ruben Jonk, Jeroen Voeten, Marc Geilen, Twan Basten and Ramon Schiffelers*
86	12:35	12:55	**Modeling RISC-V processor in IP-XACT** *Esko Pekkarinen and Timo Hämäläinen*
98	12:55	13:15	**KETCube - the Universal Prototyping IoT Platform** *Jan Bělohoubek, Jiří Čengery, Jaroslav Freisleben, Aleš Hamáček and Petr Kašpar*

ASHWPA **Advanced Systems in Healthcare, Wellness and Personal Assistance**
Chair: **Radovan Stojanovic**
Session Duration: **14:30-15:30**

	[START-TIME]	[END-TIME]	
123	14:30	14:50	**SEEK: SIP-based Emergency Embedded frameworK supports elderly and disabled to perform emergency calls** *Foteini Andriopoulou, Anastasios Fanriotis and Theofanis Orphanoudakis*
161	14:50	15:10	**MATISSE: A Smart Hospital Ecosystem** *Christos Zachariadis, Terpsichori-Helen Velivassaki, Theodore Zahariadis, Konstantinos Railis and Helen C. Leligou*
22	15:10	15:30	**A Novel Low-Complexity VLSI Architecture for an EEG Feature Extraction Platform** *Dakila Serasinghe, Duvindu Piyasena and Ajith Pasqual*

WiP **DSD - Work in Progress**
Chair: **Karl-Erwin Grosspietsch**
Session Duration: **16:00-17:30**

	[START-TIME]	[END-TIME]	
WiP6	16:00	16:10	**On the White-Box Cryptography: Design and Integration of High Performance & Lightweight Encryption** *Agamemnon Antoniadis, Nicolas Sklavos*
WiP1	16:10	16:20	**Integration of Partial Models of Multi-Agent Systems through Abstraction** *Marina Rantanen Modeer, Sebastian Engell*
WiP2	16:20	16:30	**Addressing the Execution Control Problem in Mixed-Criticality Systems** *Dávid Juhász, Axel Jantsch*
WiP3	16:30	16:40	**Scenario-aware Reconfigurable Convolutional Neural Networks (SA-RCNN) Implementation on FPGA** *Kun-Chih (Jimmy) Chen, Ya-Wei (Connie) Huang*
WiP4	16:40	16:50	**A Secure Scalable Dual-Field Multiplier for ECC** *Ievgen Kabin, Dan Kreiser, Zoya Dyka, Peter Langendoerfer*
WiP5	16:50	17:00	**Highly Integrated Low-Complexity Ultra Sound Beamformer with Dynamic Focussing** *Oscal T.-C. Chen, Yu-Zhi Ma; Guo-Zua Wu, Chih-Chi Chang*
WiP7	17:00	17:10	**An Efficient Signal Processing Technique for Phased Arrays in Satellite Communications** *Ehsan Haj Mirza Alian, Mohsen Raeis Zadeh, Hossein Gharaei Garakani, Safieddin Safavi-Naeini*
WiP8	17:10	17:20	**Feasable Wearable System for Research, Development and Education on Stress Monitoring** *Radovan Stojanovic, Andrej Skraba, Davorin Kofjac*
WiP9	17:20	17:30	**Features of the Penetrating Radiation Effect on the Electronic Components Characteristics for Aerospace Vehicles Data Processing Systems** *A. Belous, M.Kutas, V.Solodukha;I. Lovshenko, V.Stempitsky*

Friday - ROOM 2

FTET **Future Trends in Emerging Technologies**
Chair: **Oliver Keszöcze**
Session Duration: **11:15-13:15**

	[START-TIME]	[END-TIME]	
64	11:15	11:45	**Exploration of the Synchronization Constraint in Quantum-Dot Cellular Automata** *Frank Sill Torres, Pedro Arthur, Geraldo Fontes, José Augusto Nacif, Ricardo Santos Ferreira, Omar Paranaiba Vilela Neto, Jeferson Chaves and Rolf Drechsler*
63	11:45	12:05	**Evaluating the Impact of Interconnections in Quantum-Dot Cellular Automata** *Frank Sill Torres, Robert Wille, Marcel Walter, Philipp Niemann, Daniel Große and Rolf Drechsler*
84	12:05	12:25	**From Ambipolarity to Multifunctionality: Novel Library of Polymorphic Gates Using Double-Gate FETs** *Jan Nevoral, Richard Ruzicka and Vaclav Simek*
24	12:25	12:45	**Towards Reversed Approximate Hardware Design** *Saman Froehlich, Daniel Grosse and Rolf Drechsler*
134	12:45	13:05	**On Designing All-Optical Multipliers using Mach-Zender Interferometers** *Sumit Sharma, Krishnendu Chakrabarty and Sudip Roy*

SDCIS **System Design for Collaborating Intelligent Systems**
Chair: **Emad Samuel Malki Ebeid**
Session Duration: **14:30-15:30**

	[START-TIME]	[END-TIME]	
142	14:30	14:50	**Classifying Acoustic Signals for Wildlife Monitoring and Poacher Detection on UAVs** *Carlo Lopez-Tello and Venkatesan Muthukumar*
33	14:50	15:10	**A Markovian Decision Process Analysis of Experienced Agents Joining Ad-Hoc Teams** *Roghayeh Heidari, Mohsen Afsharchi and Reza Khanmohammadi*
104	15:10	15:30	**Identity and Access Management with Blockchain in Electronic Healthcare Records** *Tomas Mikula and Rune Hylsberg Jacobsen*

ML-IoT **Machine Learning Driven Technologies and Architectures for Intelligent Internet of Things**
Chair: **Farshad Farouzi**
Session Duration: **16:00-17:30**

	[START-TIME]	[END-TIME]	
ML-IoT1	16:00	16:30	**A Machine Learning Driven IoT Solution for Noise Classification in Smart Cities** *Yasser Alsouda, Sabri Pllana and Arianit Kurti*
ML-IoT2	16:30	17:00	**Experimental Study of the Algorithm Selection Hardness in Computer Vision** *Martin Lukac, Nadira Izbassarova, Albina Li and Michitaka Kameyama*
ML-IoT3	17:00	17:30	**A Safe Traffic Network Design and Architecture, in the Context of IoT** *Angeliki Kalapodi, Nicolas Sklavos, Ioannis Zaharakis and Achilles Kameas*

Friday - ROOM 3

EPDSD **European Projects in Digital System Design**
Chair: **Francesco Leporati**
Session Duration: **11:15-13:15**

	[START-TIME]	[END-TIME]	
82	11:15	11:45	**Invited talk - PRYSTINE - PRogrammable sYSTEms for INtelligence in automobilEs** *Norbert Druml, Georg Macher, Michael Stolz, Eric Armengaud, Daniel Watzenig, Christian Steger, Thomas Herndl, Marcus Hennecke, Andreas Eckel, Anna Ryabokon, Alfred Hoess, Sumeet Kumar and Herbert Roedig*
14	11:45	13:15	**TUTORIAL - Resource Management for Mixed-Criticality Systems on Multi-Core Platforms with focus on Communication** *Robin Arbaud, Dávid Juhász and Axel Jantsch*

MCSDIA **Mixed Criticality System Design, Implementation and Analysis**
Chair: **Mikel Azkarate-Askatsua**
Session Duration: **14:30-15:30**

	[START-TIME]	[END-TIME]	
174	14:30	14:50	**Functional Test Environment for Time-Triggered Control Systems in Complex MPSoCs using GALI** *Razi Seyyedi, Sören Schreiner, Maher Fakih, Kim Grüttner and Wolfgang Nebel*
173	14:50	15:10	**Exploring Power and Throughput for Dataflow Applications on Predictable NoC Multiprocessors** *Kathrin Rosvall, Tage Mohammadat, George Ungureanu, Johnny Öberg and Ingo Sander*
5	15:10	15:30	**A Reliable Statistical Analysis of the Best-Fit Distribution for High Execution Times** *Xavier Civit, Joan Del Castillo and Jaume Abella*

Poster Session

Wednesday - Coffee Break 16:30-17:00
& Thursday - Coffee Break 11:00-11:30

MAIN	*17*	**Flexible and Resource Efficient FPGA-based Quad Data Rate Memory Interface Design for High-Speed Data Acquisition Systems** *Nizam Ayyildiz*
MAIN	*26*	**Design and Implementation of an HCI based Peer to Peer APDU Protocol** *Lukas Gressl, Ulrich Neffe and Christian Steger*
MAIN	*56*	**Visualization of Memory Map Information in Embedded System Design** *Mikko Teuho, Esko Pekkarinen and Timo Hämäläinen*
MAIN	*111*	**A Versatile PCM-based Circuits Emulator and its Use on Implementing Linear Algebra Functions** *Anastasios Petropoulos and Theodore Antonakopoulos*
MAIN	*122*	**Embedded Operating System Optimization through Floating to Fixed Point Compiler Transformation** *Daniele Cattaneo, Antonio Di Bello, Stefano Cherubin, Federico Terraneo and Giovanni Agosta*
MAIN	*128*	**Attack Surface Modeling and Assessment for Penetration Testing of IoT System Designs** *Yasamin Mahmoodi, Sebastian Reiter, Alexander Viehl, Oliver Bringmann and Wolfgang Rosenstiel*
SDCIS	*146*	**Development of Autonomous Drones for Adaptive Obstacle Avoidance in Real World Environments** *Arne Devos, Emad Ebeid and Poramate Manoonpong*
ASAASIT	*16*	**Design and Implementation of Low-Cost LK Optical Flow Computation for Images of Single and Multiple Levels** *Shen-Fu Hsiao and Chen-Yen Tsai*
DCPS	*15*	**A Heuristic for Variable Re-Entrant Scheduling Problems** *Roel van der Tempel, Joost van Pinxten, Marc Geilen and Umar Waqas*
DCPS	*47*	**Building Distributed Co-simulations using CoHLA** *Thomas Nägele, Jozef Hooman and Jack Sleuters*
DCPS	*139*	**RailCheck: A WSN-based system for condition monitoring of railway infrastructure** *Jan Sramota and Amund Skavhaug*
DCPS	*151*	**Co-simulation Framework for Control, Communication and Traffic for Vehicle Platoons** *Amr Ibrahim, Chetan Belagal Math, Dip Goswami, Twan Basten and Hong Li*
MCSDIA	*7*	**Virtual Switch Supporting Time-Space Partitioning and Dynamic Configuration for Integrated Train Control and Management Systems** *Hongjie Fang and Roman Obermaisser*
MCSDIA	*124*	**Design Space Exploration for Mixed-Criticality Embedded Systems considering Hypervisor-based SW Partitions** *Vittoriano Muttillo, Giacomo Valente and Luigi Pomante*
ASHWPA	*90*	**Towards Spectral Pulse Oximetry independent of motion artifacts** *Alejandro Von Chong, Mehdi Terosiet, Aymeric Histace and Olivier Romain*
ASHWPA	*103*	**Toward an OFDM-based Technique for Electrochemical Impedance Spectroscopy** *Edwin De Roux, Mehdi Terosiet, Florian Kolbl, Aymeric Histace and Olivier Romain*
ASHWPA	*125*	**Design and Evaluation of a Low Power CGRA Accelerator for Biomedical Signal Processing** *Helder Avelar and João Canas Ferreira*
AHSA	*40*	**On the Importance of Analysing Microarchitecture for Accurate Software Fault Models** *Johan Laurent, Vincent Beroulle, Christophe Deleuze, Florian Pebay-Peyroula and Athanasios Papadimitriou*
AHSA	*50*	**Correlation Power Analysis Distinguisher Based on the Correlation Trace Derivative** *Petr Socha, Vojtěch Miškovský, Hana Kubátová and Martin Novotný*
AHSA	*54*	**Feasibility of FPGA accelerated IPsec on cloud** *Markku Vajaranta, Vili Viitamäki, Arto Oinonen, Timo Hämäläinen, Ari Kulmala and Jouni Markunmäki*
AHSA	*59*	**Exploiting Phase Information in Thermal Scans for Stealthy Trojan Detection** *Maxime Cozzi, Jean-Marc Galliere and Philippe Maurine*
AHSA	*107*	**On the Design of a Processor Working Over Encrypted Data** *Thomas Hiscock, Olivier Savry and Louis Goubin*
AHSA	*154*	**Low-temperature data remanence attacks against intrinsic SRAM PUFs** *Nikolaos Athanasios Anagnostopoulos, Tolga Arul, Markus Rosenstihl, André Schaller, Sebastian Gabmeyer and Stefan Katzenbeisser*
AMDL	*20*	**Inter-patient ECG classification using deep convolutional neural networks** *Janne Takalo-Mattila, Jussi Kiljander and Juha-Pekka Soininen*
FTET	*67*	**Optimization of Circuits for IBM's five-qubit Quantum Computers** *Gerhard Dueck, Anirban Pathak, Md. Mazder Rahman, Anindita Banerjee and Abhishek Shukla*

All posters shall be put to the poster walls during lunch break on Wednesday. They shall be removed during lunch break on Thursday.
Posters are presented during 2nd coffee break on Wednesday 16:30-17:00 and during 3rd coffee break on Thursday 11:00-11:45.
There is no template for poster presentation.
Recommended format: A0 portrait (height: 1189 mm, width: 841 mm)
Cardboard size is 100 cm width x 200 cm height.
Stickers will be available on site.