21th Euromicro Conference on Digital System Design

Prague, Czech Republic, August 29th – 31st, 2018

DSD 2018

SPECIAL SESSION ON "Dependability, Testing, and Fault Tolerance in Digital Systems (DTFT)"

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Special Session Scope

The Euromicro Conference on Digital System Design (DSD) addresses all aspects of (embedded, pervasive and high-performance) digital and mixed HW/SW system engineering, covering the whole design trajectory from specification down to micro-architectures, digital circuits and VLSI implementations. It is a forum for researchers and engineers from academia and industry working on advanced investigations, developments and applications. It focuses on today and future challenges of advanced embedded, high-performance and cyber-physical applications; system and processor architectures for embedded and high-performance HW/SW systems; design methodology and design automation for all design levels of embedded, high-performance and cyber-physical systems; modern implementation technologies from full custom in nanometer technology nodes, through FPGAs, to MPSoC infrastructures.

Every designed system has to be tested several times during its life-time - during its design, production, and its in-field operation. The need for testing strictly depends on the actual use of the system, if the system can be repaired or not, and on the requirements for the system, e.g., if the system must be dependable, fault-tolerant, etc. The design must reflect these requirements. The special session on "Dependability, Testing, and Fault Tolerance in Digital Systems" (DTFT) addresses emerging issues, hot problems, new solution methods and their hardware and software implementations in all fields of digital and analog/mixed-signal system dependability and testing. It is especially focused on testing, dependability, and fault-tolerance of SoC based designs and modern embedded applications.

Papers on any of the following and related topics can be submitted to the special session:

- Diagnosis & testing of embedded systems, SoC and NoC testing
- Memory and CPU testing
- Analog, mixed-signal and RF, IDDQ and current testing
- Built-In Self-Test: off-line BIST and on-line BIST, test compression methods
- Testability analysis, design for testability
- Error detection and correction, on-line testing, design of checkers
- Design of dependable (robust) circuits and systems, error mitigation techniques
- Defect/fault tolerant architectures (SoCs, NoCs, embedded systems)
- FPGA based fault tolerant systems, partial/full reconfiguration based methods
- Fault injection techniques, fault simulation/emulation
- Dependability modeling, dependability analysis and validation
- Formal approaches in fault tolerant systems design
- System diagnosis
- Dependable design in practical applications

Submission Guidelines

Authors are encouraged to submit their manuscripts to https://easychair.org/conferences/?conf=dsd2018. Should an unexpected web access problem be encountered, please contact the Program Chair by email (dsd2018@easychair.org).

Each manuscript should include the complete paper text, all illustrations, and references. The manuscript should conform to the IEEE format: single-spaced, double column, US letter page size, 10-point size Times Roman font, up to 8 pages. In order to conduct a blind review, no indication of the authors' names should appear in the manuscript, including references.

CPS, Conference Publishing Services, publishes the (ISI indexed) DSD Proceedings, available worldwide through the IEEE Xplore Digital Library. Extended versions of selected best papers will be published in a special issue of the ISI indexed *"Microprocessors and Microsystems: Embedded Hardware Design"* Elsevier journal.

Important Dates

Deadline for paper submission: April 15th 2018
Notification of acceptance: May 15th 2018
Camera ready papers: June 15th 2018

More Information (web pages)

DSD 2018: http://dsd-seaa2018.fit.cvut.cz/dsd/
Euromicro: www.euromicro.org